# Project Integrated circuits:

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Indholdsfortegnelse

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## Introduction

This project is made for me to learn about the differential operational amplifiers. I will try to design after some criteria, then testing and following up on if I managed to meet the requirements.

## Calculation

Et billede, der indeholder tekst, Font/skrifttype, hvid, design

Automatisk genereret beskrivelseEt billede, der indeholder tekst, Font/skrifttype, nummer/tal, linje/række

Automatisk genereret beskrivelseEt billede, der indeholder tekst, Font/skrifttype, hvid, linje/række

Automatisk genereret beskrivelseEt billede, der indeholder tekst, Font/skrifttype, skærmbillede, kvittering

Automatisk genereret beskrivelseStarting with some of the criterias:   
   
I can regulate this with the current and with the size of the transistor.



This sets up some criterias, that I can place on the parts of the circuits, coming up.

So let me go through what I currently know.

### Step 1. Common mode range

#### Input circuit

##### Requirements

,

##### Equations

##### Tests

#### Output circuit

##### Requirements

##### Equations

##### Tests

#### Step 1. Tail current circuit

##### Requirements

##### Equations

##### Tests

Et billede, der indeholder diagram, linje/række, Teknisk tegning, Plan

Automatisk genereret beskrivelseTo start it off, let me look at some common mode voltage ranges:   
For m5 it’s a diode, and for that follows:   
   
And as   
   
Then  
   
   
Giving headroom:   
   
Using that for the upper bound of the input transistor:   
   
   
   
   
   
   
  
Then the upper bound of has been found.

Now for the lower bound.   
   
   
   
Giving headroom:

So my common mode input range:

### Step 2. Size calculation for input / output, then source

#### Input circuit

##### Requirements

,

#### Et billede, der indeholder tekst, diagram, Font/skrifttype, skærmbillede Automatisk genereret beskrivelseEquations

##### Tests

Et billede, der indeholder tekst, skærmbillede, Kurve, linje/række

Automatisk genereret beskrivelse

And then

So for this dummy circuit I managed to preserve a current of about 50uA, while keeping high voltage at the drain of M1 ensuring that M1 can be in saturation.

#### Output circuit

##### Requirements

##### Equations

##### Tests

#### Tail current circuit

##### Requirements

##### Equations

##### Tests

Still assuming that , then assuming that the load capacitance is about negligible compared to the transistor current of M2   
   
Just solving for one of the input transistors. The other I say is approximately the same as the other. But creating a relationship to the tail transistor.

But VD4 also sets the lower bound for the common mode voltage range…  
   
Ensuring that:   
   
   
  
Then the maximum value VD4 is

Ensuring the input transistor:   
   
   
   
   
Then the tail transistor:

Solving for the pmos transistors aswell.

The maximum value of makes for .

Setting the transistor dimension equal for the input layer, output layer, and current source layer.  
And then I have:

Et billede, der indeholder tekst, diagram, Plan, skematisk

Automatisk genereret beskrivelseTesting it I only manage 2.4uA through M4.   
Et billede, der indeholder tekst, skærmbillede, Kurve

Automatisk genereret beskrivelse

So I’ll be going back to testing some of the paths.

So far:

### Step 3. Input / output / source errors

#### Input circuit

##### Requirements

,

##### Equations

##### Tests

#### Output circuit

##### Requirements

##### Equations

##### Tests

#### Tail current circuit

##### Requirements

##### Equations

##### Tests

Is the tail current capable of running 100uA?

Et billede, der indeholder diagram, tekst, linje/række, Plan

Automatisk genereret beskrivelsePlotting with the current size configuration, I get that about is able to flow through.

Maybe I derived the formula the wrong way?

I derived it from   
   
Let me retry:

Et billede, der indeholder skærmbillede, tekst, display/skærm/fremvisning, Multimediesoftware

Automatisk genereret beskrivelse   
   
   
That’s a completely different value. Maybe that will work.

That helped, but not quite there.   
Fiddling with the values I get that   
, gets 98.7uA ≈ 100uA.

Implementing it into the Output / input directly makes itail go from 98 -> 82. Just implementing it onto the input layer with VDD directly gets itail go form 98 -> 93.   
This is due to not being met. The voltage is seen to be 0,084V.  
Adjusting the ratio of the input transistor from 0,563 -> 0,7 made all the current run through and satisfy the saturation criteria.

Et billede, der indeholder tekst, skærmbillede, diagram, nummer/tal

Automatisk genereret beskrivelseNow adding the pmos network onto it:

The saturation criteria isn’t meet, and its due to the pmos network. Let me tweak their value a little.

I actually realized, that even though I found to be 450, 100 worked almost just as great. Changing the ratio of the pmos didn’t do much else. Adjusting V1 a little more, gives this little more headroom. The saturation criteria for the tail transistor is met for

### Step 4. Biasing resistor

#### Input circuit

##### Requirements

,

##### Equations

##### Tests

#### Output circuit

##### Requirements

##### Equations

##### Tests

#### Tail current circuit

##### Requirements

##### Equations

##### Tests

Now cobbling this to my current mirror source.   
I’ve set , VG4 = 0,66.   
   
   
   
 by a little bit, and that forces changes in the circuit.

Et billede, der indeholder tekst, skærmbillede, diagram, linje/række

Automatisk genereret beskrivelse



Lifting input transistor size ratio , and increasing the bias transistor to 9000Ω fixes this.

*Now I’ve solved all this for the upper bound, but how does this hold when put at the lower bound?*Recalling boundary equation 5.   
And recalling that the minimum value of

Let me test it:

### Step 5. Common mode range in practice.

#### Input circuit

##### Requirements

,

##### Equations

##### Tests

I’ve calculated my Vin to be satisfied by about 800mV, but in practice, this didn’t work.  
Testing at Vin = 1,2V.   
Testing it where it barely satisfies the common mode range criteria.   
It barely reaches saturation. 60uA isn’t 100 but this will have to do.

Et billede, der indeholder tekst, skærmbillede, diagram, linje/række

Automatisk genereret beskrivelse

#### Output circuit

##### Requirements

##### Equations

##### Tests

#### Tail current circuit

##### Requirements

##### Equations

##### Tests

## Finished circuit.

### Common mode range

I solved for , but in practice, even at 1,2V, saturation wasn’t meet.   
At about 1.2V. The drain current is 60uA.   
At about 1.3V. The drain current is 82uA  
At about 1.4V. The drain current is 97uA so it seems like saturation is meet.

In reality, I only reached a Vin common mode range of 0.3V.

### Gain

#### Et billede, der indeholder skærmbillede, linje/række, Kurve, Font/skrifttype Automatisk genereret beskrivelseDifferential gain.



#### Et billede, der indeholder skærmbillede, tekst, Font/skrifttype, linje/række Automatisk genereret beskrivelseCommon mode gain

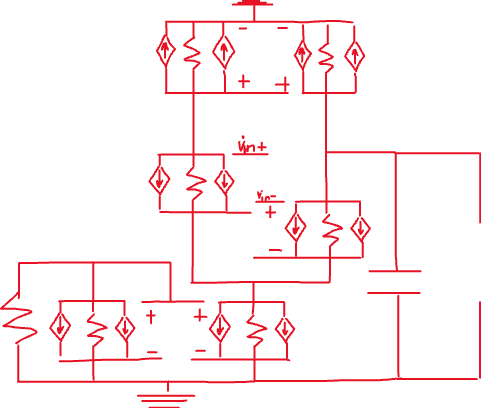
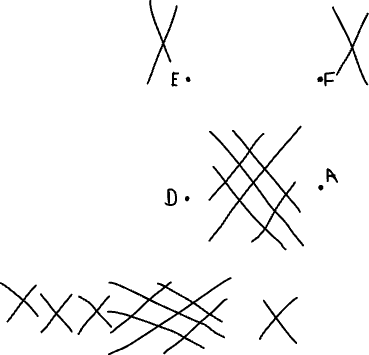


### CMRR

### Et billede, der indeholder skærmbillede, Kurve, tekst, Grafiksoftware Automatisk genereret beskrivelseGBW

I get

### Dominant pole



Let me start with the equation A.

*Ligningen løses for i\_M2 vha. WordMat.*

Substituting into equation D.

Substituting back into into equation 1.



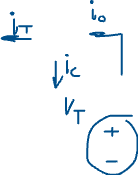
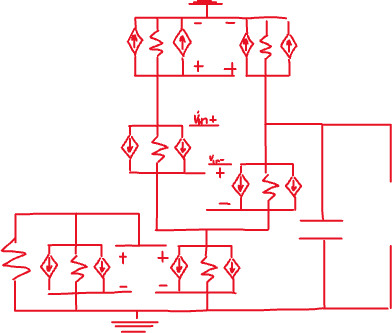
Substituting into equation E.



Now for the final equation.



Oops, I forgot the load capacitor. The current is then not from the source.   
   
And the output resistance is



Et billede, der indeholder skærmbillede, Kurve, linje/række, Font/skrifttype

Automatisk genereret beskrivelse



I’ve simplified the channel length modulation to be zero. But for my plots, they use the default values:

========  
   
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Et billede, der indeholder tekst, Font/skrifttype, hvid

Automatisk genereret beskrivelseSeems weird. Let me retry with the given Rout.   
I’ve gotten this differential gain formula.   
Assuming   
   
   
   
Minimum value of Ids2 and Ids6. What I observe of at the pmos drain is Isd = -Ids.

There might be a dominant pole at around s ≈ 0, but it might also just be a wrong value.   
I believe more in the second pole calculated.   
=============  
   
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### Et billede, der indeholder skærmbillede, Kurve, linje/række, Font/skrifttype Automatisk genereret beskrivelseSlew rate

I was expected to get   
   
My

## Conclusion

I designed for a differential operational amplifier. The main parameter for design where the sizes of the transistor. I designed for the source network, input network and the output network, with their sizes being equal, respectively. I calculated for the right values, simulated, saw differences in what I expected and adjusted accordingly. I got saturation to work for all transistors at 1,7V, but then adjusting to lower values, saturation wasn’t fully fulfilled.  
But it was a design, and I might think about designing it different next time.   
I then compared the criteria to what my circuit could achieve.